REMARKS

Claim Rejections Under 35 U.S.C. § 112

Claim 30 recited the limitation "the mode register" in line 5. Claim 31 recited the limitation "the mode register" in line 3. Claims 30 and 31 have been amended to change "mode register" to "input signal" to correct a typographical error in the claims.

Claims 30-34 were rejected under 35 U.S.C. § 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. The amendments to claims 30 and 31 render this rejection moot.

Claim Rejections Under 35 U.S.C. § 102

Claims 1-44 were rejected under 35 U.S.C. § 102(e) as being anticipated by Nobunaga et al. (U.S. Patent No. 6,304,510). Applicant strongly traverses this rejection.

First, the rejection contains only a blanket assertion that all 44 claims of the present application are anticipated by the reference, without addressing how. Since Applicant has not been given a chance to respond to more than a cursory outline of how the Nobunaga et al. reference is being applied to the claims, Applicant submits that even if another Office Action is provided in this application, that it would be improper for it to be a Final Office Action, since Applicant has not been afforded the opportunity to address any specific rejections.

Further, Applicant submits that Nobunaga et al. does not contain each and every element of the claims, as is required to support a rejection under 35 U.S.C. § 102(e). Nobunaga et al. is directed generally to memory device address decoding. In contrast, the present application is directed generally to configuration of the number of banks in a memory, and the associated structure and methods to accomplish that.

With reference to the entire pending claim set and the rejections thereof, Applicant submits that nowhere in Nobunaga et al. is any mention made at all of configuring the number of banks in a memory. In fact, nowhere in Nobunaga et al. is there made any mention of any memory that does not have four banks. The Office Action itself asserts that Figure 1 shows either four or eight banks. In fact, Figure 1 and the accompanying text of the Nobunaga et al. specification clearly and unambiguously show and describe four banks, namely banks 104, 106, 108, and 110. There is no mention of reconfiguring the number of banks, and there is certainly

no mention of the same physical structure being configurable into a different arrangement of banks, as is the subject generally of the pending claims. Further, the assertion that status register 130 is a "mode register" that performs the functions of the mode register identified and recited in the present claims is wholly unsupported by the specification and figures of Nobunaga et al.

The "mode register" 130 of Nobunaga et al. is identified as a command execution logic including a status register 134 and an identification register 136, neither of which operate to "configure the addressable banks" as is recited in claim 1, to "configure the array in response to a program state of the mode register, wherein the mode register defines a number of addressable banks of the array" as is recited in claim 4, or routing a selected address to either the row or bank address decoder "in response to data stored in the mode register" as in claim 9. Further, Nobunaga et al. contains no teaching or disclosure of configuring the addressable banks in any way. Claims 1, 4, and 9 are allowable. Claims 2-3, 5-8, and 10-11 depend from and further define one of patentably distinct claims 1, 4, or 9, and are also allowable.

Claim 12 recites "logic circuitry" that works with the address signal circuitry to route a selected address input connection to the row or bank address decoder in "in response to the logic circuitry." This is not present anywhere in Nobunaga et al. As such, claim 12 is allowable. Claims 13-15 depend from and further define patentably distinct claim 12, and are also allowable.

Claim 16 recites "a decode circuit" and address circuitry that configures the addressable banks "in response to a program state of the input signal." Once again, Nobunaga et al. contains no mention or teaching whatsoever of configurable banks or a system containing the elements of the claim. Claim 16 is allowable. Claims 17-20 depend from and further define patentably distinct claims 16, and are also allowable.

Claims 22 and 30 each recite that the "input signal defines a number of addressable banks of the array." Claim 27 recites address circuitry "to configure the addressable banks in response to a program state of the external input signal." Claims 38 and 42 each recite that "the address circuitry configures a number of addressable banks of a memory cell array." As has been repeatedly shown above, Nobunaga et al. contains no such teaching or disclosure. As such, claims 22 and 27 are allowable. Claims 23-26, 28-29, 39-41, and 43-44 depend from and further define one of patentably distinct claims 22, 27, 38, and 42, and are also allowable.

Claim 35 recites that "the address signal circuitry routes a selected on of the plurality of address input connections to either the row or bank address decoder in response to data decoded by the decode circuit." Once again, there is no such teaching in Nobunaga et al. Claim 35 is

allowable. Claims 36-37 depend from and further define patentably distinct claim 35, and are also allowable.

Claims 16-29 and 35-44 were rejected under 35 U.S.C. § 102(e) as being anticipated by Zitlaw et al. (U.S. Patent No. 6,549,468). Applicant also strongly traverses this rejection.

First, the rejection contains only a blanket assertion that claims 16-29 and 35-44 of the present application are anticipated by the reference, without addressing how. Since Applicant has not been given a chance to respond to more than a cursory outline of how the Zitlaw et al. reference is being applied to the claims, Applicant submits that even if another Office Action is provided in this application, that it would be improper for it to be a Final Office Action, since Applicant has not been afforded the opportunity to address any specific rejections.

Further, Applicant submits that Zitlaw et al. does not contain each and every element of the claims, as is required to support a rejection under 35 U.S.C. § 102(e). Zitlaw et al. is directed generally to address scrambling in memories. In contrast, the present application is directed generally to configuration of the number of banks in a memory, and the associated structure and methods to accomplish that.

There is no mention at all anywhere in Zitlaw et al. of any configuration of the number of memory banks in a memory, as is recited in all of the claims 16-29 and 35-44 as discussed in greater detail above. In fact, nowhere in Zitlaw et al. is there made any mention of any memory that does not have four banks. The Office Action itself asserts that Figure 1 shows either four or eight banks. In fact, Figure 1 and the accompanying text of the Zitlaw et al. specification clearly and unambiguously show and describe four banks, namely banks 104, 106, 108, and 110. There is no mention of reconfiguring the number of banks, and there is certainly no mention of the same physical structure being configurable into a different arrangement of banks, as is the subject generally of the pending claims. Zitlaw et al. contains no teaching or disclosure of configuring the addressable banks in any way.

CONCLUSION

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2203.

Respectfully submitted,

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